IN THE CLAIMS

1. (Twice Amended) A nonvolatile memory cell array comprised of a plurality of EEPROM memory cells, each cell comprising:

a semiconductor substrate having a top surface;

a vertical MOS transistor formed by alternating N-type and P-type doped layers in said substrate and wherein a well is etched into said substrate through said alternating N-type and P-type layers such that said alternating layer surround said well, said well having a floating gate of conductive material formed therein which is self aligned so as to have only components that are orthogonal to said top surface of said substrate and so as to not extend laterally beyond edges of said well and insulated from and overlying said alternating N-type and P-type layers by a layer of gate insulating material;

a word line contact comprising a layer of conductive material formed on said substrate so as to extend down into said well and overlie said floating gate but insulated therefrom by an insulation layer; and

a bit line contact comprising a layer of conductive material formed [on] all portions of which are formed above said top surface of said substrate so as to be in electrical contact with the drain region of said vertical MOS transistor formed in said substrate at the location of each vertical MOS transistor in said array.

2. (Twice Amended) A nonvolatile memory cell array comprised of a plurality of nonvolatile memory cells, each memory cell comprising:

a semiconductor substrate having a top surface and having a drain region of a first conductivity type formed [therein and having a] below said top surface so as to have

a surface coincident with said top surface of said substrate and suitable to act as a drain region of a vertical MOS transistor;

a buried layer channel region in said semiconductor substrate doped so as to have a second conductivity type having the majority of charge carriers therein of a different polarity than said first conductivity type and suitable to act as a channel of a vertical MOS transistor formed in said substrate;

a source region [of] below said top surface of said semiconductor substrate and below said channel region, said source region being doped so as to have said first conductivity type;

a recessed gate window in the form of a well etched in said semiconductor substrate through said first layer of insulating material, said well being deep enough to penetrate through said channel region and into said source region such that at least some portion of the side wall or sidewalls of said trench are bordered by said source, drain and channel regions;

an insulating layer covering the bottom of said well;

a gate insulating layer formed on the sidewall of said well;

a self aligned floating gate comprising a conductive material formed within said well on said gate insulating layer so as to only have a conductive component on said sidewall of said well and not on the bottom of said well no portion of said self aligned floating gate extending [not extend] beyond the edges of said well;

an insulating layer formed over said self aligned floating gate so as to electrically isolate said floating gate from all surrounding structures, said floating gate having a dimension suitable so as to overlie at least said channel region;

a word line comprising conductive material deposited so as to extend into said

well far enough to overlie at least a portion of said floating gate; and

a second layer of insulating material formed so as to [insulate at least a portion of] completely cover said word line; and

a bit line all portions of which are formed [over] above said top surface of said semiconductor substrate so as to make contact with at least a portion of said drain region at each said memory cell but insulated from said word line by said second layer of insulating material.

3. (Amended) A nonvolatile memory cell array comprised of a plurality of EEPROM memory cells, each cell comprising:

a semiconductor substrate having a top surface;

a vertical MOS transistor formed by a first three-dimensional layer of N-type conductivity [and having] formed within said substrate so as to have a surface coincident with [the] said top surface of said substrate and forming a drain region of said vertical MOS transistor, a second layer of P-type conductivity within said substrate and adjacent to and underlying said first layer relative to [the] said top surface of said substrate and forming a channel region of said vertical MOS transistor, and a third layer of N-type conductivity within said substrate and adjacent to and underlying said second layer and forming a source region of said vertical MOS transistor, and having a well etched into said substrate so as to penetrate through said first and second layers and at least partially through said third layer, said well having a floating gate of conductive material formed therein which is self aligned so as to not extend laterally beyond edges of said well and so as to have only a conductive component on the walls of said well but not on the bottom thereof, [and] said self aligned floating gate overlying said first, second and third